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A 32-site neural recording probe fabricated by DRIE of SOI substrates

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Abstract
An all-dry silicon-etch based micromachining process for neural probes was demonstrated in the manufacture of a probe with a 32-site recording electrode array. The fork-like probe shafts were formed by double-sided deep reactive ion etching (DRIE) of a silicon-on-insulator (SOI) substrate, with the buried SiO_2 layer acting as an etch stop. The shafts typically had the dimensions 5 mm $\times$ 25 μm $\times$ 20 μm and ended in chisel-shaped tips with lateral taper angles of 4°. An array of Ir electrodes, each 100 μm^2, and Au conductor traces were formed on top of the shafts by e-beam evaporation. An accompanying interconnect solution based on flexible printed circuitry was designed, enabling precise and flexible positioning of the probes in neural tissue. SEM studies showed sharply defined probes and probe tips. The electrical yield and function were verified in bench-top measurements in saline. The magnitude of the electrode impedance was in the 1 MΩ range at 1 kHz, which is consistent with neurophysiological recordings.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

It is believed that a key to the understanding of the nervous system is to make simultaneous observations of the activity of a large number of cells [1]. Probes that can penetrate neural tissue and insert a large number of recording sites, while tissue damage is kept to a minimum, are thus needed. Micro system technology (MST) is well suited to this end, and several MST based neural probe concepts have been presented.

A wet silicon-etch based process was demonstrated early [2], and later a combination of wet silicon etching and a p^{++} diffused etch stop was used to define fork-like probe shapes [3]. Neural probes combined with on-chip integrated circuitry were also demonstrated [4, 5]. In a later approach, a combination of patterned deep reactive ion etching (DRIE) of the wafer front side, and blank wet silicon etching of the back side was used to form the probe shapes [6]. Two-dimensional arrays of recording electrodes, distributed on fork-like silicon probe structures are the most common approach, but the distribution of the recording sites on the tips of a 'bed-of-nails' structure has also been shown [7]. Alternatives to silicon have also been presented, e.g. flexible polyimide-based devices [8, 9].

Nevertheless, there is still room for improvements on previous processes and designs, in order to optimize the trade-off between different requirements. Requirements to be considered are, e.g., the possibility of independently tailoring the shape of the probe tips for reduced tissue dimpling, the inclusion of a thicker support structure to facilitate handling of the thin probes after processing, increased electrode density through reduced linewidths, process uniformity, yield, complexity, manufacturability, and in the end cost.

An all-dry silicon-etch based process where the buried oxide layer of a silicon-on-insulator (SOI) substrate acts as an etch stop, was introduced by us in [10], and independently by Cheung *et al* in [11]. The process avoids the visual

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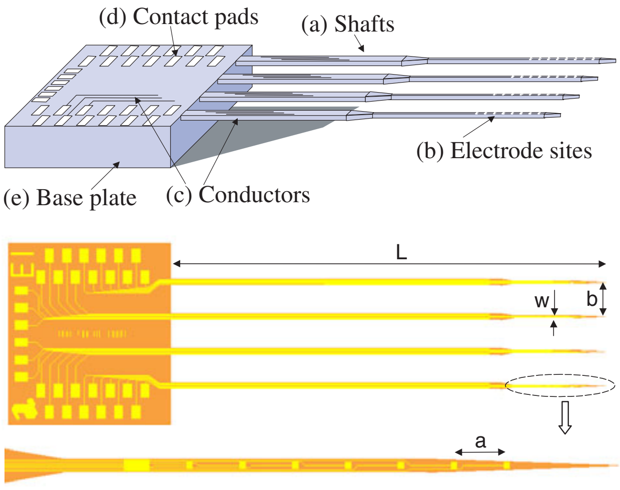

Figure 1. Schematic drawing of the probe structure described in the text (not to scale) and a typical CAD layout.

end conditions, which should improve upon uniformity and manufacturability. Double-sided lithography and etching allow a thicker base plate to be part of the design. In this work, we demonstrate the process in the fabrication of neural recording probes with 32-site recording arrays. A double metal layer process allows a larger number of electrodes and conductors to be fitted on narrower shafts.

In the MST field, the design of an appropriate and cost-effective interconnect and packaging solution is often of nearly equal importance as the device design itself. Here, the silicon device is accompanied by a tailor-made connector solution based on flexible printed circuitry, enabling precise and flexible positioning of the probes with micromanipulators during recordings in neural tissue.

2. Design

2.1. Silicon probes

Referring to figure 1, the main design elements of the probe structure are: (a) fine and pointed Si shafts for penetration and insertion into neural tissue, (b) microelectrode sites of Ir distributed over the outermost section of the shafts, (c) fine and narrowly spaced Au conductor traces, ending in (d) Au contact pads for external electrical interconnection using wire bonding, and (e) a thicker Si base plate as a support for the contact pads, to allow easy handling of the probes.

In a typical design, there are four shafts with eight electrode sites each, eight shafts with four sites each, alternatively one shaft with 32 sites. The shaft width (w) is 25 μm at the outermost section, widening to usually 75 μm at the base plate. The shaft thickness is targeted to ~20 μm, but can be varied with the SOI wafer specification. The shaft length (L) is typically between 4 mm and 7 mm and the

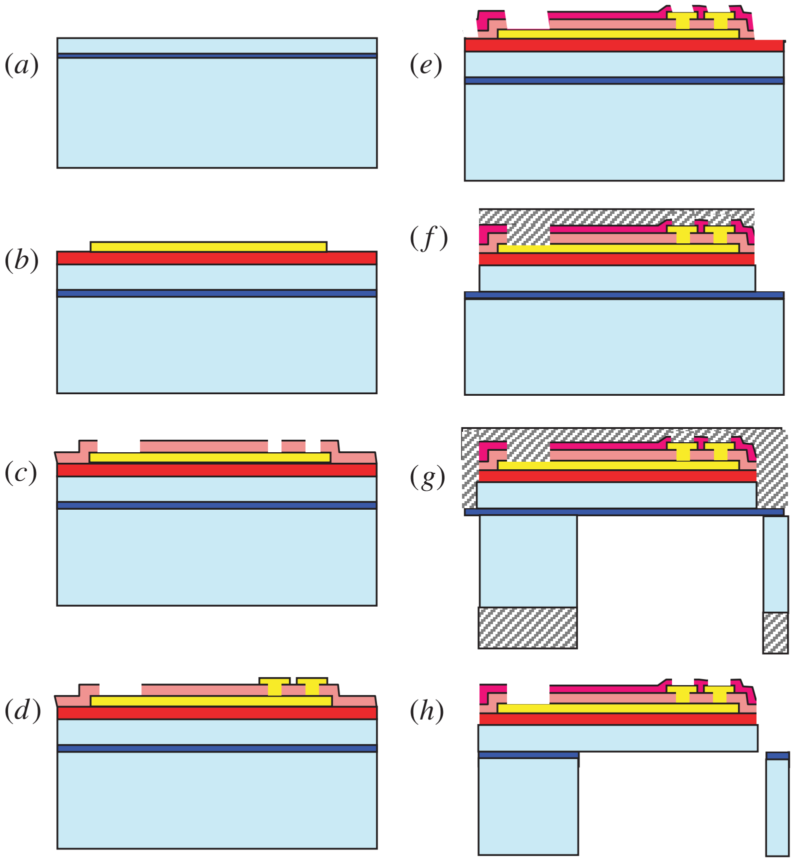

Figure 2. Schematic illustration of the fabrication process described in the text (not to scale). (*a*) SOI wafer, (*b*) SiN deposited, litho 1, Ti/Au deposited and lift off, (*c*) SiN deposited, litho 2 and nitride etch, (*d*) litho 3, Ti/Ir deposited and lift off, (*e*) SiN deposited, litho 4 and nitride etch, (*f*) litho 5, SiN etch and front side Si etch, (*g*) litho 6 and back side Si etch and (*h*) oxide etch and resist strip.

shaft c/c distance (b) is 200–400 μm, for different designs. The recording electrode sites are 10 μm $\times$ 10 μm and are distributed with a 50–200 μm pitch (a).

The lateral tip taper angle is designed to 4°. The optimization of neural probe tips with respect to tissue penetration properties and dimpling is not self-evident, see [12] for a discussion. Factors to be considered are, e.g. tip angle, tip radius, tip geometry (conical, chisel-like, pyramid-like, . . .), sharp cutting edges, shaft width and thickness, shaft roughness, surface chemistry, and insertion velocity. The present manufacturing process will result in chisel-shaped tips. The effect of very small tip taper angles (in spite of the tip not being sharpened in the third dimension) will be the subject of future investigations, but is motivated by a set of as yet unpublished experiments.

2.2. Interconnect and packaging

In order to interface the small probe chips with the comparatively larger amplifier system, a flexible printed circuit (FPC) solution was designed. The front end of the FPC was designed to fit the silicon probe chip and its bond pad positions. The back end was tailored to mate with the preamplifier connector (Molex 52559, 0.5 mm pitch, SMT, Zero Insertion Force type). The FPC was made of a polyimide foil with conductor traces of copper and Ni/Au metal at the contact pads. The dimensions of the FPC are 125 mm $\times$ 9 mm $\times$ $\sim$65 μm. A stiffening of glass fibre epoxy (FR4) was employed at the front end of the FPC to create a rigid support under the probe chip, and to function as an interface to standard micromanipulators. A thinner stiffening of polyester gives to the back end the thickness required by the connector. A commercial manufacturer [13] produced the flexible circuits, according to our designs.

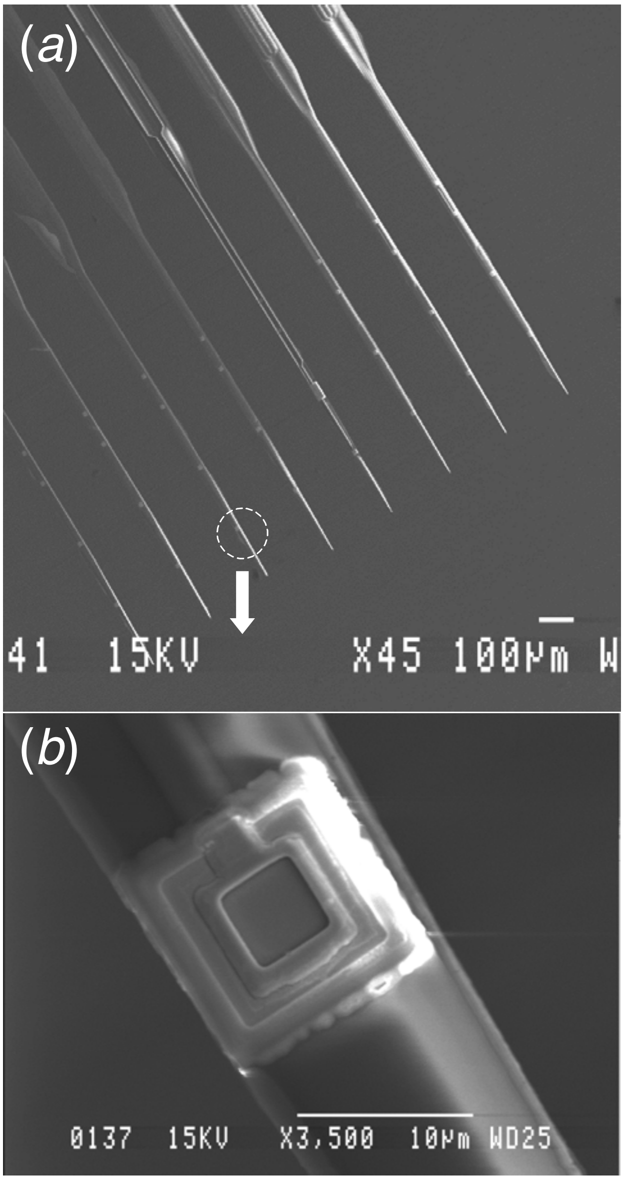

Figure 3. Scanning electron micrograph of (a) a silicon probe with 8 shafts $\times$ 4 electrodes and (b) close-up of a 10 μm $\times$ 10 μm Ir electrode site.

3. Fabrication process

The silicon probe fabrication process is outlined in figure 2 and in the following text (italic letters refer to figure 2): (a) The probes were manufactured on silicon-on-insulator (SOI) substrates (Shin Etsu, 100 mm ϕ, 525 μm Si/1.5 μm SiO_2/20 μm Si). (b) A PECVD silicon nitride film (1 μm) was deposited as an isolation layer. Ti/Au ($\sim$500 Å/2500 Å) was e-beam evaporated and patterned with a photo-resist lift-off process, to form conductor traces. Five times reduction step-and-repeat projection lithography was used with down to 1 μm linewidths and spacing. (c) A second silicon nitride layer (0.5 μm) was deposited as an intermediate dielectric. Via holes were opened to the Au-layer using reactive ion etching (RIE) through a resist mask. (d) Ti/Ir ($\sim$300 Å/3500 Å) was e-beam evaporated and patterned with lift-off, to form the electrode sites. (e) A final silicon nitride layer (0.5 μm) was deposited as a protective layer. Windows were opened to the Au bond pads and the Ir electrode sites using RIE. The nitride covers the edges of the metal patterns for increased reliability in wet working environments. (f) With a resist mask the remaining nitride layer was first RIE etched, after which the top silicon layer was etched 20 μm down to the buried oxide in an inductively coupled plasma deep reactive ion etching equipment (ICP DRIE, Surface Technology Systems). (g) A thick resist was spun on the wafer front side for protection. A double-sided mask alignment (Karl Suss MA6) was used to pattern a thick resist on the wafer backside, which was etched the full 525 μm down to the buried oxide in the ICP DRIE. (h) The shafts were released by first etching the buried oxide in buffered HF, followed by a final resist strip.

In variations of the basic process outlined above, we have also worked with thermal silicon oxide as the first dielectric layer to achieve a stress-compensated thin film stack, and platinum as an alternative to iridium for the electrode metal.

After processing, the probe chips were mounted on FPCs with glue (cyanoacrylate). An ultrasonic wire bonder (West Bond 7400) was used to connect the bond pads on the chip with the pads on the FPC with gold wires (25 μm ϕ). An epoxy

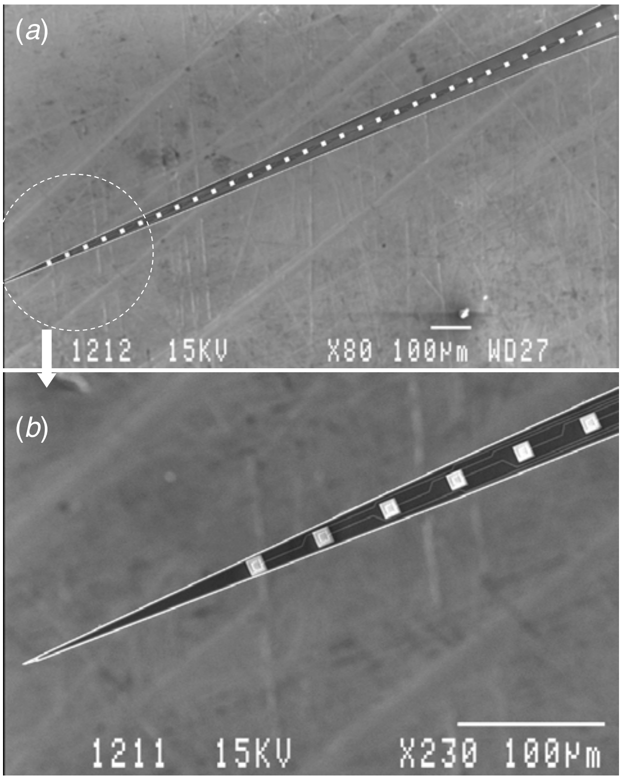

Figure 4. Scanning electron micrograph of (*a*) a silicon probe with 1 shaft × 32 electrodes and (*b*) close-up of a probe tip designed with 4° taper angle. The interconnect lines shown are 1 μm wide.

Figure 5. A neural probe chip mounted on a flexible printed circuit, wire-bonded and glob-top protected (right). A FPC without the glob-top cover is also shown (middle). The back end of the FPC was designed to mate with a 32-pin ZIF connector (shown left).

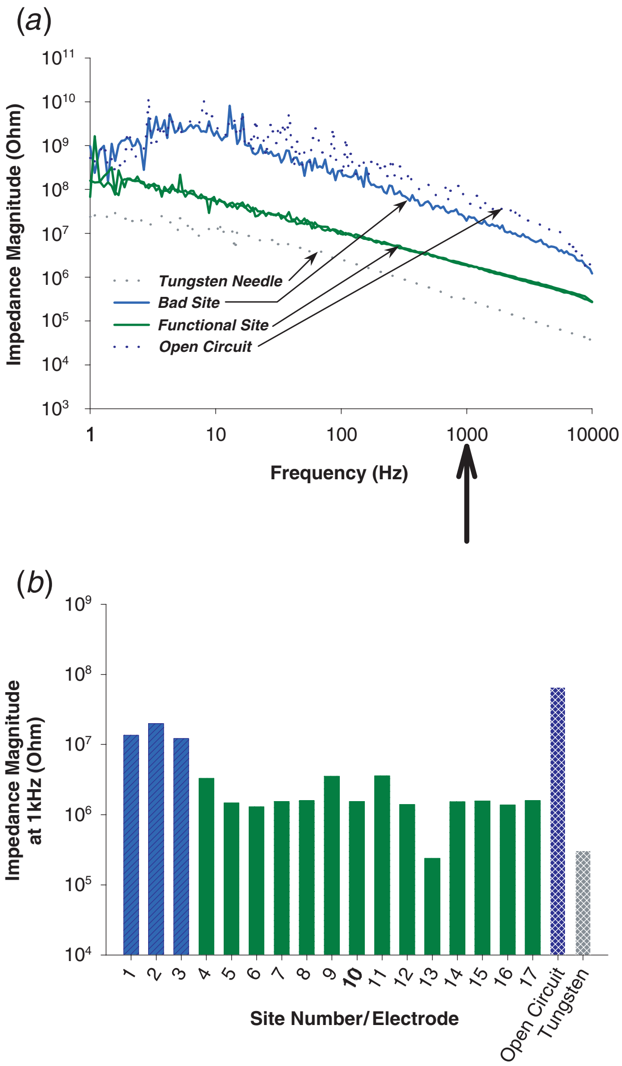

Figure 6. (*a*) Typical impedance magnitude spectra of two Ir sites on a silicon probe ('Functional Site'). For comparison a site with wire bond failure ('Bad Site'), a commercial tungsten needle electrode (AM-systems, type 5753) and the upper limit of measurement are also shown. (*b*) Impedance magnitudes at 1 kHz of a larger sample of sites on the same probe. Sites 1–3 show wire bond failures, number 13 is a non-standard electrode designed with a factor 10 larger area. The other sites show nominal 1.5 MΩ impedance. (To enable quick evaluation, the probe under test was not glob-top protected, which accounts for the wire bonds accidentally broken during handling.)

glob top (Emerson & Cuming, Amicon 50300/400 series) was applied to protect the bond wires from mechanical damage and wet working environments.

4. Experimental results

Figures 3 and 4 show scanning electron micrographs of the results of the micromachining process. The DRIE process in combination with stepper lithography enabled tight control of the structural dimensions. Electrodes and conductors could be packed close to the probe shaft edges and the probe tip taper design was well reproduced. Figure 5 shows the main parts of the developed interconnect solution.

Bench-top measurement set-ups were used to verify the electrical functionality of the probes after processing. Qualitatively we have been able to verify a satisfactory process yield, where a majority of the tested electrode sites transmits electrical signals. Quantitatively, the electrode impedance is a parameter of prime interest, since it influences the thermal (Johnson) noise and the ability to record small neural signals. For evaluation a rapid 3-point electrode impedance measurement technique was used, which is a modified

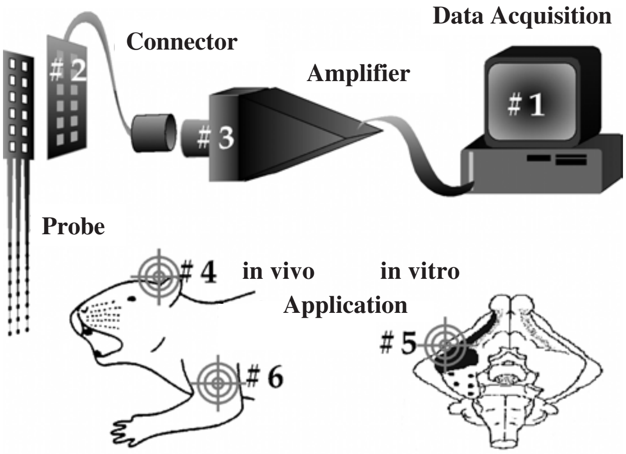

Figure 7. Overview of a complete recording system (1–3) and areas of application experiments (4–6) in the EU project VSAMUEL: 1. Data acquisition system, hardware and software; 2. custom designed connectors and batch fabricated multisite microelectrode probes; 3. discrete and modular multi-channel amplifier; 4. cerebellum; 5. cortex; 6. peripheral nerves.

version of the rapid 2-point electrode impedance measurement technique described in [14]. Use of a 3-point measurement scheme eliminates the effect of the counter-electrode impedance on the overall impedance measurement. The technique yields the electrode impedance spectrum between ~1 Hz and 10 kHz with short 1–10 s measurements. Shortly, a bandwidth limited noise current is passed through the test electrode and a large Ag/AgCl counter electrode is immersed in 0.9% saline. The current through the test electrode and the voltage drop across the test electrode and a separate Ag/AgCl reference electrode is measured. Fast Fourier transforms are taken of the appropriately sampled and windowed voltage and current waveforms and the empirical transfer function is estimated. This estimate directly yields the impedance spectrum of the test electrode.

A typical set of impedance spectra is shown in figure 6. We found that the Ir recording sites were of the order of 1.5 MΩ at 1 kHz. This impedance is comparable to those of needle electrodes suitable for single unit recording, and the results are in good agreement with previously published data from thin film Ir microelectrodes [15]. If required, the Ir electrode impedance levels can be further reduced by oxidation by potential cycling (‘activation’) [15, 16].

5. Conclusions

A manufacturing process for micromachined neural probes, based on double-sided deep reactive ion etching of silicon-on-insulator substrates was demonstrated in the design and manufacture of probes with 32 recording electrodes, distributed on one to eight fine and pointed Si shafts. The process resulted in sharply defined probes and probe tips. The electrical yield was verified and the magnitude of the electrode impedance was shown to be consistent with neural recordings. The process appears to be attractive with respect to process complexity, uniformity and manufacturability. The interconnect and packaging solution, based on flexible printed circuitry provides a user-friendly interface, well adapted to the requirements of neuroscientists.

Work is under way to scale up the probe design to an increased number of electrodes. Furthermore, this work is part of a larger consortial effort to develop a complete system for neural recordings, and to demonstrate the system in different application experiments [10] (cf figure 7). The systems approach as well as the collaboration between several hardware developer groups and neuroscience user groups are expected to bring added value to the neural probe concept.

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