

A 32-site Neural Recording Probe Fabricated by Double-Sided Deep Reactive Ion Etching of Silicon-on-Insulator Substrates

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Abstract

A neural probe with a 32-site electrode array was fabricated using an all-dry Si etch based micromachining process.

The fork-like probe shafts were formed by double-sided deep reactive ion etching (DRIE) of a silicon-on-insulator (SOI) substrate, with the buried SiO₂ layer acting as an etch stop. The shafts typically had the dimensions 5 mm x 25 μm x 20 μm and a tip taper of 4°. An array of Ir electrodes, each 100 μm², and Au conductor traces were formed by e-beam evaporation.

SEM studies showed sharply defined probes and probe tips. The function was verified in bench-top measurements in saline. The magnitude of the electrode impedance was in the 1 MW-range @ 1 kHz, which is consistent with neural recordings.

1. Introduction

It is believed that a key to the understanding of the nervous system is to make

simultaneous observations of the activity of a large number of cells. Probes that can penetrate neural tissue and insert a large number of recording sites, while tissue damage is kept to a minimum, are thus needed. Micro System Technology is well suited to this end, and several MST based neural probe concepts have been presented during the years.

For example, a wet Si etch based process, where the probe shape is defined by a p⁺⁺ diffused etch stop was demonstrated early [1]. In a later approach, a combination of patterned deep reactive ion etching (DRIE) of the wafer front side, and blank wet Si etching of the back side was used to form the probe shapes [2].

Nevertheless, there is still room for improvements on previous processes and designs, in order to optimize the trade off between different requirements, such as: the possibility to independently tailor the shape of the probe tips for reduced tissue dimpling, the inclusion of a thicker support structure to facilitate handling of the thin

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probes after processing, process uniformity, yield, complexity, manufacturability, and in the end cost.

In this work we introduce an all-dry Si-etch based process where the buried oxide layer of an SOI substrate acts as an etch stop, thus avoiding visual end conditions, which should improve upon uniformity and manufacturability. Double-sided lithography and etching allows a thicker base plate to be part of the design.

2. Design

Referring to figure 1, the main design elements of the probe structure are: (a) Fine and pointed Si shafts for penetration and insertion into neural tissue. (b) Microelectrode sites of Ir distributed over the outermost section of the shafts. (c) Fine and narrowly spaced Au conductor traces, ending in (d) Au contact pads for external electrical interconnection using wire bonding. (e) A thicker Si base plate as a support for the contact pads, and to allow easy handling of the probes.

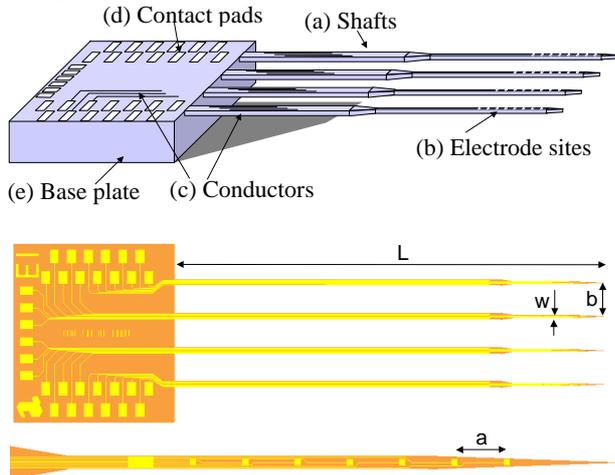


Figure 1. Schematic 3D drawing of the probe structure (not to scale) and a typical CAD layout.

In a typical design, there are four shafts with eight electrode sites each, alternatively eight shafts with four sites each. The shaft

width (w) is $25\ \mu\text{m}$ at the outermost section, widening to $75\ \mu\text{m}$ at the base plate. The shaft thickness is targeted to $\sim 20\ \mu\text{m}$, but can be varied with the SOI wafer specification. The shaft length (L) is $5\ \text{mm}$ and the shaft c/c distance (b) is $400\ \mu\text{m}$. The tip taper angle is 4° . The electrode sites are $10\ \mu\text{m} \times 10\ \mu\text{m}$ and are distributed with $100\ \mu\text{m}$ pitch (a). The parameters L , b and a as well as the number of shafts were varied within a full wafer layout.

3. Fabrication process

The silicon probe fabrication process is outlined in figure 2 and in the following paragraph (bold letters refer to figure 2).

(a) The probes were manufactured on silicon-on-insulator (SOI) substrates (Shin Etsu, $100\ \text{mm}\ \phi$, $525\ \mu\text{m}\ \text{Si}/1.5\ \mu\text{m}\ \text{SiO}_2/20\ \mu\text{m}\ \text{Si}$). (b) A PECVD silicon nitride film ($1\ \mu\text{m}$) was deposited as an isolation layer. Ti/Au ($\sim 500\ \text{\AA}/2500\ \text{\AA}$) was e-beam evaporated and patterned with a photo-resist lift-off process, to form conductor traces. Step-and-repeat projection lithography was used with down to $1\ \mu\text{m}$ linewidth and spacing. (c) A second silicon nitride layer ($0.5\ \mu\text{m}$) was deposited as an intermediate dielectric. Via holes were opened to the Au-layer using reactive ion etching (RIE) through a resist mask. (d) Ti/Ir ($\sim 300\ \text{\AA}/3500\ \text{\AA}$) was e-beam evaporated and patterned with lift-off, to form the electrode sites. (e) A final silicon nitride layer ($0.5\ \mu\text{m}$) was deposited as a protective layer. Windows were opened to the Au bond pads and the Ir electrode sites using RIE. The nitride covers the edges of the metal patterns for increased reliability in wet working environments. (f) With a resist mask the remaining nitride layer was first RIE etched, after which the top silicon layer was etched $20\ \mu\text{m}$ down to the buried oxide in an inductively coupled plasma deep re-

active ion etching equipment (ICP DRIE, Surface Technology Systems). **(g)** A thick resist was spun on the wafer front side for protection. Double-sided mask alignment was used to pattern a thick resist on the wafer backside, which was etched the full 525 μm down to the buried oxide in the ICP DRIE. **(h)** The shafts were released by first etching the buried oxide in buffered HF, followed by a final resist strip.

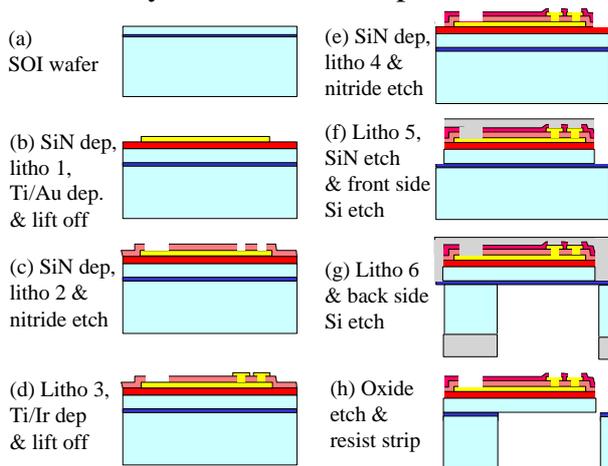


Figure 2. Schematic illustration of the fabrication process (not to scale).

4. Experimental results

Figures 3 and 4 show scanning electron micrographs of the results of the micro-machining process.

Bench-top measurement setups were used to verify the electrical functionality of the probes after processing. Qualitatively we have been able to verify a satisfactory process yield, where a majority of the tested electrode sites transmits electrical signals.

Quantitatively, the electrode impedance is a parameter of prime interest, since it influences the thermal noise and the ability to record small neural signals. For evaluation a rapid 3-point electrode impedance measurement technique was used, which is a modified version of the rapid 2-point technique described in [3].

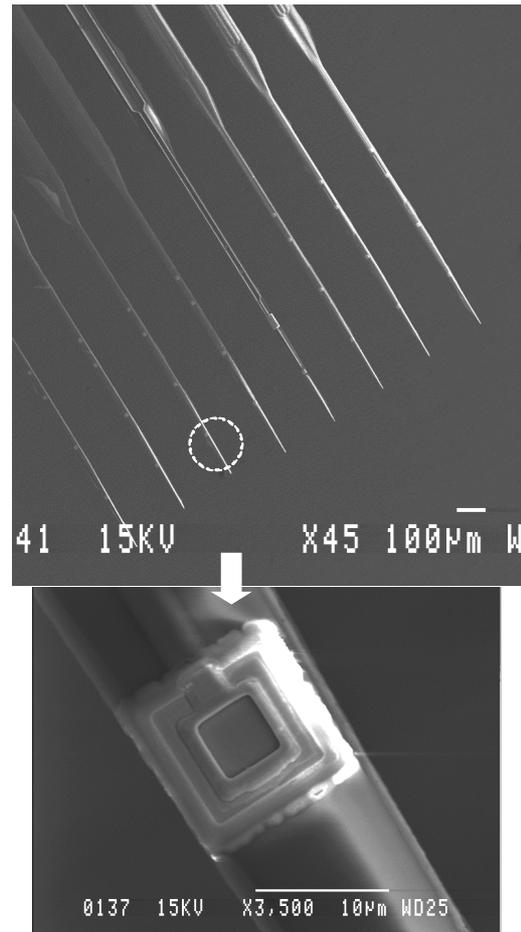


Figure 3. SEM of silicon probes with 32 microelectrodes (top) and a $10\ \mu\text{m} \times 10\ \mu\text{m}$ Ir electrode site (bottom).

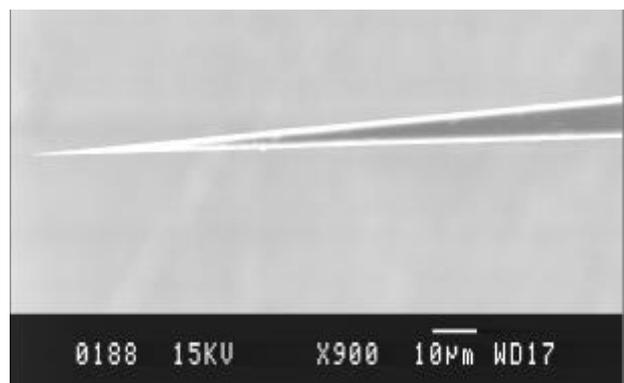


Figure 4. SEM of a probe tip designed with 4° taper angle.

The technique yields the impedance spectrum between ~ 1 Hz and 10 kHz with short 1-10 second measurements. A bandwidth limited noise current is passed through the test electrode and large Ag/AgCl counter electrode immersed in 0.9

% saline. The current through the test electrode and the voltage drop across the test electrode and a separate Ag/AgCl reference electrode is measured. Fast Fourier Transforms are taken of the appropriately sampled and windowed voltage and current waveforms and the empirical transfer function estimated, which directly yields the impedance spectrum of the test electrode. A typical set of impedance spectra is shown in figure 5 (dashed line indicates the limit of the measurement system, upper curves are from non-functional sites).

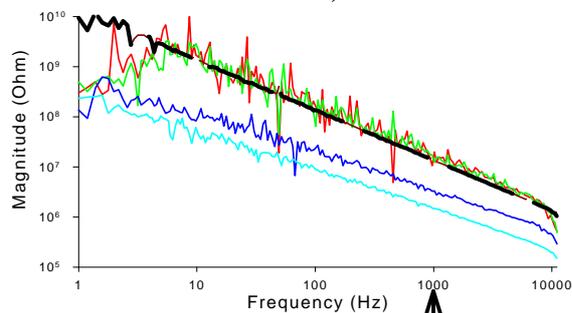


Figure 5. Typical impedance spectra.

We found that the recording sites were on the order of 1.5 M Ω at 1 kHz. This impedance is comparable to those of needle electrodes suitable for single unit recording.

5. Conclusions

A novel manufacturing process for micromachined neural probes, based on double-sided deep reactive ion etching of silicon-on-insulator substrates was presented. Probes with 32 recording electrodes distributed on four to eight fine and pointed Si shafts were fabricated using this process.

The process resulted in sharply defined probes and probe tips. The electrical yield was verified and the magnitude of the electrode impedance was shown to be consistent with future neural recordings. The process appears attractive with respect to complexity, process uniformity and manufacturability. Work is under way to scale up

the design to an increased number of electrodes, longer shafts, and to optimize the thin films with respect to intrinsic stress.

Furthermore, this work is part of a larger effort to develop a complete system for neural recordings, and to demonstrate the system in different application experiments [4] (figure 6). The systems approach as well as the collaboration between several hardware developer groups and neuroscience user groups is expected to bring added value to the neural probe concept.

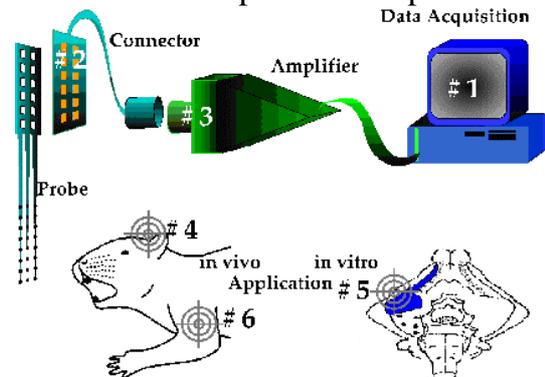


Figure 6. Overview of a complete recording system (#1-3) and areas of planned application experiments (#4-6).

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References

- [1] K. Najafi, Wise, K.D., Mochizuki, T., "A High-Yield IC-Compatible Multichannel Recording Array", *IEEE Trans. Electron Devices*, **ED-32**, 1985, pp. 1206-1211.
- [2] D. T. Kewley et al., "Plasma-etched neural probes", *Sensors and Actuators*, **A58**, 1997, pp. 27-35.
- [3] K. Yoshida, Inmann, A., Haugland, M.K., "Measurement of complex impedance spectra of implanted electrodes", *4th Ann. Conf. of the Int. Functional Electrical Stimulation Society*, Sendai, Japan, 1999, pp. 267-269.
- [4] U.G. Hofmann, De Schutter, E., Yoshida, K., de Curtis, M., Norlin, P., "On the design of multi-site microelectrodes for neuronal recordings", *Proc. VDE World Microtechnologies Congress (MICRO.tec 2000)*, Hannover, VDE Verlag, 2000, pp. 283-288.